Programming general-purpose chips, sharing photomask real estate, or even dispensing with masks altogether are options for cost control in low-volume chips.

Masking Costs

By Kristin Lewotsky

Amid all of the fuss about development costs for new generations of lithography, it's easy to lose sight of a major problem currently facing the industry—photomask cost. Mask sets, which can consist of 30 or 40 individual masks, currently run about $750,000, and experts expect them to reach $1 million in the near future. For manufacturers producing high-volume chips, it's not as big of an issue, with quantity reducing the cost to perhaps $0.10 to $1 per device. "They can afford to spend the money on the masks," says Rista Puhakka, vice president at VLSI Research (Santa Clara, CA). "They do it grudgingly, but they do it."

The problem arises with the low-volume chips, primarily application-specific integrated circuits, which can be produced in lots as small as 25 wafers. If you split $1 million across 25 wafers, that's $400,000 per wafer; assume 400 dies per wafer and you've got a mask cost of $100 per die. "That's not feasible in any circumstances," says Puhakka.

But the reality is worse. "We talk about a $1 million mask set, but there's also usually $3 million to $4 million of additional design cost that goes into that," says VLSI's Dan Hutcheson. "Now I've got a $4 million to $5 million cost of designing a chip. How do I build a hundred of those?"

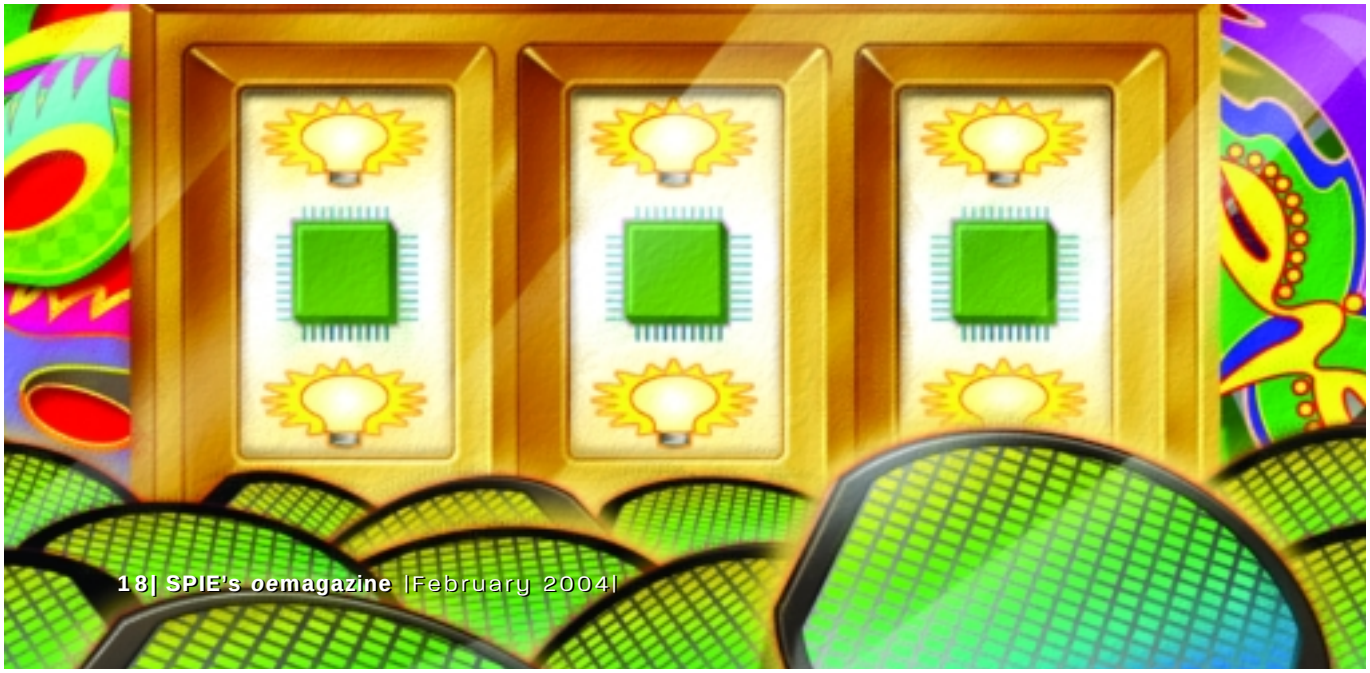
The primary cost driver for photomasks is the write time. Depending on the design, a mask can require from five to 40 hours to write. "That's tying up a piece of equipment that may cost $15 million," says Tom Blake, vice president of marketing at DuPont Photomasks (Round Rock, TX). Add mask inspection, another two to five hours, also with costly equipment, and the problems mount. "If there are defects on the mask and you can't repair them, you have to start over again," says Blake.

The industry is beginning to explore a number of options to address the small-volume issue. The first is to substitute high-volume chips like field-programmable gate arrays that can be programmed to perform the same tasks. "They're not as fast," says Hutcheson, "but when you get down to low unit volumes it's about the only way you can afford to do it unless you're willing to pay thousands of dollars per chip."

Another method is to gang designs from multiple customers on a single mask substrate, a method typically attractive for prototyping. The economies of scale here are multifold, with savings on substrates and mask writer setup time. Most important, it spreads the write cost among several projects. Instead of one customer paying $1 million for a mask set containing four dies of one design, for example, four customers will each contribute $250,000 of the mask write cost and as a group receive a mask with one die of each of their designs.

Dispensing with masks entirely is yet another approach. Direct-write lithography has been around for several years. It suffers from the same issues as mask writing, though—throughput and cost. "Moore's Law is not working in your favor," observes Hutcheson. "There are people that manage to make it work on a limited scale. It's just that it's never been mainstream, and I don't believe it'll be mainstream."

One way or another, the industry needs to find a solution. Puhakka, for one, remains philosophical. "It's relatively hard to address that issue of mask cost, assuming we will continue on Moore's Law. It's going to create changes in industry structure in favor of more general-purpose chips." Puhakka doesn't look at the change as negative for the industry, but simply as another level in semiconductor evolution. "It's something that's going to happen," he says. "Just take it as it is." **oe**



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